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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,796	06/01/2001	Craig L. Stevens	10001.000600 (NVLS 379)	4156

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EXAMINER	
KIELIN, ERIK J	

ART UNIT	PAPER NUMBER
2813	13

DATE MAILED: 12/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/872,796	Applicant(s) STEVENS ET AL.	
	Examiner Erik Kielin	Art Unit 2813	

-- Th MAILING DATE of this communication appears on th cov r sh et with the correspond nce addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5,9* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This action responds to IDS submissions of 29 August 2001 and 1 June 2001, and the election filed 31 October 2002.

Information Disclosure Statement

1. The information disclosure statement filed 29 August 2001 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. No copies of the listed references have been provided.

Moreover, the reference listed last additionally fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because some of the references have not been provided with dates in accordance with 37 CFR 1.98(b)(5). Also the MPEP 609 states,

> "Each publication must be identified by publisher, author (if any), title, relevant pages of the publication, and date and place of publication. The date of publication supplied must include at least the month and year of publication, except that the year of publication (without the month) will be accepted if the applicant points out in the information disclosure statement that the year of publication is sufficiently earlier than the effective U.S. filing date and any foreign priority date so that the particular month of publication is not in issue." (Emphasis added.)

The IDS has been placed in the application file, but only the references initialed by Examiner have been considered. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the

requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Drawings

2. Figures 1A, 1B and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. (See specification, p. 4, lines 16-18.) See MPEP § 608.02(g).

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **1**-13 and **17**-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,251,759 B1 (**Guo** et al.) in view of US 6,270,582 B1 (**Rivkin** et al.).

Regarding independent claims 1 and 17, **Guo** discloses a wafer processing system comprising:

a load lock **114** (Fig. 1);

a transport module having a load chamber **113** (called "buffer chamber" in Guo), a transfer chamber **101**, and a pass-through chamber **122** (additionally called "transition chambers" in Guo col. 4, line 19) located between the load chamber and the transfer chamber, the load chamber being coupled to the load lock;

an intermediate process module **124** (called "transition chambers" in Guo col. 4, line 19) coupled to the load chamber and the transfer chamber (as further limited by instant claim 20);

a first set of process modules **116**, **118**, **121** coupled to the load chamber;

a second set of process modules **104**, **106**, **108**, **110** coupled to the transfer chamber.

Guo does not indicate if the load lock is a single-wafer load lock having a single-wafer water-cooled pedestal (as further limited by instant claims 8, 18, and 19).

Rivkin teaches a single-wafer load lock (title) for a multi-chamber semiconductor wafer process module having a water-cooled, single-wafer pedestal **136** (Fig. 3; col. 6, lines 1-4, lines 37-47).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use the single-wafer load lock of **Rivkin**, in the process system of **Guo** to enable additional processing mot typically provided in a load-lock, as is taught to be beneficial in **Rivkin** (Abstract and Summary of Invention).

Regarding claims 2, **Guo** shows process module **118** connected to the load chamber 113 (the first set of process modules) may be a pre-clean module (col. 4, line 7).

Regarding claims 3 and 4, **Guo** shows process module **121** connected to the load chamber 113 (the first set of process modules) may be a physical vapor deposition (PVD) or chemical vapor deposition (CVD) module (col. 4, lines 49-52).

Regarding claim 6, **Guo** shows process module **104** connected to the transfer chamber 101 (the second set of process modules) is a chemical vapor deposition (CVD) module (col. 4, lines 64-66).

Regarding claims 10, 11, and 21, **Guo** discloses that it is known for the intermediate process module **122** to be configured as either a cooling station or a pre-clean module (col. 1, 45-48; col. 4, line 47).

Regarding claim 12, **Guo** shows the intermediate process module **124** is configured as a PVD chamber.

Regarding claims 5, 7, 9, and 13, **Guo** does not specifically indicate that the second set of process modules (those on the transfer chamber **101**) include a pre-clean module (claim 5) or a PVD module (claim 7), or that the intermediate process module **122**, **124** may be configured as a degas module (claim 9) or a CVD module (claim 13). Note however, that **Guo** teaches the benefits of configuring one of the intermediate chambers **122**, **124** as a PVD module (col. 3, lines 43-50). Additionally, **Guo** teaches that the ordering of process modules is "illustrative" (col. 3, lines 60-63), and that cluster tools include a variety of ordered tools depending upon the process being performed (col. 1, lines 30-48), and also that metallization cluster tools include CVD, PVD, pre-clean and degas modules, among others (col. 2, lines 34-59 and through out the specification and figures). This suggests to one of ordinary skill in the art that the arrangement is a matter of design choice to best suit a given processing steps to be performed in a

semiconductor wafer. Moreover, it has been held that mere rearrangement of parts is evidence of obviousness. *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to have a pre-clean module or PVD module in the second set of process modules and to have a degas and pre-clean modules as intermediate modules, in order to optimize the process throughput for a given process, as taught by **Guo** and according to precedent. Moreover, Applicant indicates that virtually any arrangement of process modules is possible, thereby teaching away from the criticality of any specific arrangement in the processing system.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 5,199,483 (**Bahng**) discloses a cooling system for wafers (Abstract).

US 5,281,320 (**Turner** et al.) teaches that the load lock volume should be minimized to accommodate a single wafer in order to reduce the amount of pumpdown required for the load lock (col. 7, lines 112-16).

US 5,789,878 (**Kroeker** et al.) states,

> "Modern semiconductor processing systems include cluster tools that integrate a number of process chambers together in order to perform several sequential processing steps without removing the substrate from the highly controlled processing environment. These chambers may include, for example, degas chambers, substrate pre-conditioning chambers, cooldown chambers, transfer chambers, chemical vapor deposition chambers, physical vapor deposition chambers, and etch chambers. The combination of chambers in a cluster tool, as well as the operating conditions and

> parameters under which those chambers are run, are selected to fabricate specific structures using a specific process recipe and process flow.
>
> Once the cluster tool has been set up with a desired set of chambers and auxiliary equipment for performing certain process steps, the cluster tool will typically process a large number of substrates by continuously passing them, one by one, through the same series of chambers or process steps. The process recipes and sequences will typically be programmed into a microprocessor controller that will direct, control and monitor the processing of each substrate through the cluster tool." (See col. 9, line 51 to col. 10, line 10.)

Moreover, **Kroeker** shows that the second set of process modules on the transfer chamber include both CVD and PVD. This provides suggestion to one of ordinary skill to order the first set, second set. intermediate, and pass-through modules for whatever processing best suits the sequence of the steps.

US Patent application 2001/0041122 A1 **(Kroeker)** teaches a single wafer load lock. (Abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 703-306-5980. The examiner can normally be reached on 9:00 - 19:30 on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Erik Kielin
December 11, 2002